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Dip Cheung

GitHub
M-Labs Git
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A software developer for the Advanced Real-Time Infrastructure for Quantum physics (ARTIQ) project, a leading-edge control system for quantum information experiments. Majored in both Computer Science and Electronic Engineering. Graduated from The Hong Kong University of Science and Technology (HKUST). Worked for M-Labs Limited from 2020 to 2022. Currently a Computer Science Master's student in University of California, Santa Barbara.

Education

Bachelor of Science, Computer Science, with an additional major in Electronic Engineering
Hong Kong University of Science and Technology, CGA: 4.102/4.3, First Class Honors — **Sep 2017 — May 2021**
Exchange Program, University of British Columbia, Average Score: 92.4% — **Jan 2020 — Apr 2020**
Master of Science, Computer Science, University of California, Santa Barbara, GPA: 4.0/4.0 — **Since Sep 2022**

Experience

Student Helper
Department of Computer Science and Engineering (CSE), HKUST — **Sep 2019 — Nov 2019**

- Student helper of 3 courses during the 2019-20 Fall: **COMP 1022P** *(Introduction to Computing with Java)*; **COMP 2011** *(Programming with C++)*; and **COMP 2611** *(Computer Organization)*.
- Responsible for: Attending the lab sessions to assist the teaching/instructional assistants (TA/IA); Answering questions from the students; Grading students' lab assignments during the lab sections.

Division of Integrative Systems and Design (ISD), HKUST — **Feb 2021 — May 2021**

- Student helper of **ISDN 4000G** *(Internet of Things: From Component Skills to System Integration)* during 2020-21 Spring. Topic includes analysis of simple DC analog circuits, signal and system analysis, source coding, channel coding and the MQTT protocol.
- Responsible for: Attending the lab sessions to assist the students to complete laboratory tasks; Answering questions from the students throughout the semester; Grading students' on various tasks throughout the semester, including laboratory tasks, written assignments, midterm exam and the final project.

Software Developer (Intern) — **Jul 2020 — Jan 2021**
M-Labs Limited

- Completed the ELEC Corporate/Co-op Final Year Project "**Firmware Development for Scientific Instruments**" during the internship, see the projects section for more details.
- Participated in the development of the driver for ENC424J600, and implement a network stack using smoltcp & embedded-nal (later merged into smoltcp-nal) and MiniMQ on the next generation firmware for Sinara Booster, an 8 channel RF power amplifier in the Sinara open hardware ecosystem.
- Assembled Sinara systems for ARTIQ, which were supplied to institutions across the world.

Software Developer — **Jun 2021 – Aug 2022**
M-Labs Limited

- Completed a port of VexRiscv cores (an implementation of the RISC-V ISA) to ARTIQ. Implemented stack overflow protection for ARTIQ firmware, and an object linker for the new ARTIQ Compiler, 3rd iteration (NAC3). See the projects section for more details.

Projects

Corporate/Co-op Final Year Project: Firmware Development for Scientific Instruments — **Jul 2020 — Dec 2020**
Supervised by: Mr. Sébastien Bourdeauducq (M-Labs), Prof. Kam Tim Woo (ECE, HKUST)

- Made a network controllable RF signal generator using Sinara hardware (Urukul & Humpback). RF signal is generated by direct digital synthesis (DDS) ICs on Urukul, controlled by an STM32H743 microcontroller programmed in Rust, connected by an iCE40 FPGA programmed using Migen and the IceStorm toolchain.
- Single-tone (simple sinusoidal) RF signals can be generated, where the frequencies and amplitudes are controllable. Modulated signal output is available. Amplitude, phase or frequency modulated signal can be generated.
- Network commands are implemented using the secured MQTT (MQTTS) protocol. It allows RF signal to be controlled by multiple device in parallel with only 1 network socket in the firmware, improved from the traditional 1-to-1 network socket using plain TCP.
- MQTTS protocol is based on the Transport Layer Security (TLS) protocol. A Rust library **"SaiTLS"** was created to implement TLS using Rust and the *smoltcp* networking stack. Common encryption algorithms such as AES-GCM and NIST P-256 are supported.
- Source code of the firmware and **SaiTLS** are available in M-Labs Git.

Port of ARTIQ to RISC-V **Jun 2021 — Sep 2021**

- Replaced the *mor1kx (OpenRISC)* cores with **VexRiscv** *(RISC-V)* cores in ARTIQ. The migration to the more popular RISC-V ISA enables support from other technologies. The full LLVM toolchain can be deployed directly to compile the runtime and kernels.
- The performance of ARTIQ using RISC-V cores improved in terms of data transfer speed. Asynchronous throughput improved by approximately 0.2 MiB/s on KC705, from 2.3 MiB/s to 2.5 MiB/s. Other metrics also showed a slight improvement from previous the OpenRISC cores in general.
- Contributions were made to other ISA dependent libraries as well, including Libfringe *(context switching)*, LLVM-Libunwind *(exception handling)* and MiSoC *(FPGA SoC builder)*.

Stack Overflow Protection in ARTIQ firmware **Sep 2021 — Oct 2021**

- Added a 4KiB long guard page for every stack memory region in the ARTIQ firmware, which includes both the spawned threads and main thread of the ARTIQ runtime, satellite manager, and kernel. (Bootloader is the only exception.)
- Exceptions are raised when the guard page are accessed, which includes reading, writing, and executing instructions.
- The implementation leveraged the privileged ISA and the Physical Memory Protection (PMP) units of RISC-V architecture. Minor contributions were submitted to the VexRiscv repository regarding the PMP logic, to improve compliance towards the corresponding RISC-V privileged specifications.

NAC3 Linker (nac3ld) **Feb 2022 — Jun 2022**

- Implemented a light-weight, minimalist's, and fast static linker for the new ARTIQ Compiler, 3rd iteration (NAC3). It links the compiled relocatable object into non-standard dynamic library. nac3ld is specifically built and optimized for ARTIQ NAC3 kernels.
- Nac3ld introduced text section relocation to the dynamic library. It reduced 1 level of indirection when accessing ARTIQ (with NAC3) kernel control registers and exposed functions. It brought around 36 ns (10%) performance improvement to the minimum sustained TTL output switching rate on KC705.
- Nac3ld substituted the LLVM linker (lld) in NAC3. It yielded an 5% improvement to ARTIQ kernel compilation speed for RISC-V targets, and minor improvements to the ARM Cortex A9 target.

Academic Awards

Dean's List **2017-18 Fall & Spring**
2018-19 Fall & Spring
2019-20 Fall
2020-21 Spring

Dean's List is awarded at the end of a regular term if a term grade average (TGA) of at least 3.7 is achieved, calculated from at least 12 credits registered.

HKUST Academic Achievement Medal **2021**

The Academic Achievement Medal is awarded to outstanding graduates in the year of graduation. Recipients must achieve an overall cumulative grade average (CGA) of at least 3.9, which includes at least 60 credits obtained at HKUST.

ELEC Best Final Year Project/Thesis Awards 2020-21 - 2nd Runner Up **2021**

Awarded by the Department of Electronic and Computer Engineering (ECE) of HKUST, in recognition of the **"Firmware Development for Scientific Instruments"** *project.*

Scholarships

University's Scholarship Scheme for Continuing Undergraduate Students **2018-19**
AEON Credit Service Scholarship **2018-19**
Fung Scholarship **2019-20**
The Joseph Lau Luen Hung Charitable Trust Scholarship **2019-20**
M-Labs Fellowship **2022-24**